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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,838	11/26/2003	Suan Jeung Boon	303.601US3	8165

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SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2813	
MAIL DATE	DELIVERY MODE
01/22/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,838	BOON, SUAN JEUNG	
	Examiner	Art Unit	
	JAMES M. MITCHELL	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,27-33 and 59-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,27-33 and 59-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/29/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed September 29, 2008.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on September 28, 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Booth et al. (U.S. 5,747,101).

5. Booth (e.g. Fig. 1-3) discloses:

(cl. 1) A method of packaging comprising: applying an adhesive (2) to a first side of a finished wafer (1), the first side of the finished wafer having at least one die (Fig. 11, step 113→step 115), the finished wafer having one or more pads used for calculating or measuring point where hole is to be formed and therefore is a datum (e.g. alignment mark/ structure in chip used to form pad, 8) on the first side, the adhesive being one or more of an elastomer applied in fluid form, a thermoplastic material, or a pressure-sensitive film (Fig. 4, step 31); controlling the application of the adhesive such that the

adhesive substantially covers the entire first side of the finished wafer as a uniform adhesive layer (Fig. 2; Col. 2, Lines 65-67) and after applying the adhesive to the first side of the finished wafer, forming an array of conductive elements (4) within the adhesive to a level substantially flush with a surface of the adhesive layer (Fig. 4, step 33 & Fig. 9), the surface being distal to the first side, to allow the adhesive to contact a support to attach the at least one die to the support at initial contact of the array of conductive elements with the support (e.g. the prior art forms the same structure as claimed and is capable of being used in the claimed manner; Fig. 14) , the array of conductive elements electrically coupled to an array of connection pads (8) on the at least one die, wherein the array of conductive elements includes a plurality of conductive elements (4), wherein the one or more datums are used to align the array of conductive elements (Fig. 9), the one or more datums disposed on the first side (e.g. top portion of wafer) such that the array does not contact the one or more datums (e.g. separated by 8);

(cl. 2) wherein forming an array of conductive elements includes: creating openings in the adhesive, the openings aligned with the array of connection pads/datum (8);
and substantially filling the openings with an electrically conductive material (Fig. 4);

(cl. 3) an array of conductive elements includes forming conductive material selected from one or more of lead-based solders, lead-free solders, conductive polymers, or conductive pastes (“paste”; CLAIM 1 of Booth).

6. Claims 27, 28, 30, 31 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith (U.S. 5,808,874)[1].

7. Smith (e.g. Fig. 1, 8) discloses:

(cl. 27) A method of packaging comprising: providing an adhesive layer, the adhesive layer being a substantially independent film- like structure (Col 6, Lines 33-40); after providing the adhesive layer (10; "elastomer"; Col. 2, Lines 50-52), forming an array of conductive elements (42; Col. 6, Lines 37-38) within the substantially independent film-like adhesive layer such the adhesive layer and the array of conductive elements form a structure essentially consisting of the adhesive layer and the array of conductive elements; and after forming the array of conductive elements within the adhesive layer, applying the adhesive layer having the array of conductive elements within the adhesive layer to a first side of a finished wafer (22; Col. 7, Lines 1-4), the first side of the finished wafer having one or more dice, to couple the array of conductive elements electrically to an array of connection pads on a first die of the one or more dice;

(cl. 28) forming an array of conductive elements within the adhesive layer includes forming openings in the adhesive layer and forming conductive material in the openings to form the array of conductive elements (Col. 6, Lines 36-40);

(cl. 30) an array of conductive elements includes forming an array of solder columns (Fig. 3, 8);

[1] Note that various other references such as Patent (e.g. U.S. 6,270,363) could have been used showing interconnects in an adhesive layer.

(cl. 31) an array of conductive elements includes forming an array of solder balls (42; Col 7, Lines 2-3);

(cl. 33) singulating the first die from the finished wafer and forming an individual flip chip package (Col. 4, Lines 38-41).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 6-9 and 59-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Booth et al. (U.S. 5,747,101) in combination with Kovac et al. (U.S . 6,133,639).

10. Booth discloses the elements stated in paragraph 5 of this office action and further singulating the wafer (12, Fig. 14 & Fig. 11, step 113), forming an individual flip chip/individual die and mounting the chip to a support providing interface with external circuitry and therefore a mother board (Fig. 11, step 115 & Fig. 14) and curing the adhesive (Col. 3, Lines 9-11), applying a dispensing apparatus (e.g. “mask screening”; CLAIM 8 of Booth) wherein the adhesive is cured prior to filling opening (Col. 2, Lines 65-67), but fails to disclose use of an elastomer material.

11. Kovac (170) utilizes an elastomer material.

12. It would have been obvious to one of ordinary skill in the art to modify the wafer package of Booth by forming its encapsulating material as an elastomer in order to accommodate CTE mismatch as taught by Kovac (Abstract).

13. With respect to the selected dimensions/shape of the adhesive of claims 65 and 66 including a chamfer is formed around the opening[2], applicant has not disclosed that the bevel shape groove is for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. As such, the claimed limitation would have been obvious to one of ordinary skill in the art, since, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

14. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Booth et al. (U.S. 5,747,101) in combination with Hoang (U.S. 6,201,301).

15. Booth discloses the elements stated in paragraph 5 of this office action, but does not disclose applying an encapsulant on its wafer's second surface.

[2] Simply an opening with a bevel shape as shown in applicant's Figure 4.

16. However, Hoang (e.g. 30a) teaches applying a protective encapsulant on a second/back surface of its semiconductor.

17. It would have been obvious to one of ordinary skill in the art to incorporate applying a protective coating to a second side of the wafer of Booth in order to provide thermal transfer and additional protection as taught by Hoang (Col. 3, Lines 51-55 & 57-60).

18. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (U.S. 5,808,874) in combination with Booth et al. (U.S. 5,747,101).

19. Smith discloses the elements stated in paragraph 7 of this office action, but does not disclose using a laser to form vias,

20. Booth (Col. 2, Line 66) teaches use of a laser cutting to form vias/openings.

21. It would have been obvious to one of ordinary skill in the art to incorporate use of a laser to the adhesive/elastomer of Smith in order to provide vias as taught by Booth (3).

22. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (U.S. 5,808,874) in combination with Yoshizawa (U.S. 5,819,406).

23. Smith discloses the elements stated in paragraph 7 of this office action, but does not appear to show applying to its adhesive layer a film with a removable backing and removing the removable backing after securing the adhesive lager to the first side of a finished wafer.

24. Yoshizawa utilizes a removable backing applied to its adhesive and removing the removable backing layer (Fig. 24A→24F).

25. It would have been obvious to one of ordinary skill in the art to incorporate with the adhesive of Smith a removable backing in order to fill holes within its adhesive as taught by Yoshizawa (Fig. 24D→24E).

26. With respect to the removable layer being taken off after attaching the adhesive to the wafer, applicant has not disclosed that the claimed sequence is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. As such, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical,. Moreover, the sequence would have been obvious, since it has been held that well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. Ex parte Rubin 128 USPQ (PO BdPatApp 1959).

Response to Arguments

27. Applicant's arguments with respect to his amended claims have been considered but are moot in view of the new ground(s) of rejection. With respect claim 27, applicant contends that Smith does not disclose it layer 10 as having an adhesive. Examiner respectfully disagrees. Smith discloses that the layer itself may cause adherence or that adhesives may be applied to layer 10 surfaces, either of which is within the borad

scope of applicant's claim. Without addressing the merits of the composition being either an elastomer/ b-stage etc. and therefore not an adhesive, the argument is moot, since applicant's claim only recites an adhesive; No specific material is claimed.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. MITCHELL whose telephone number is (571)272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 21, 2009
/James M. Mitchell/
Examiner, Art Unit 2813